**AMD**

Am79571/Am79573/Am79574

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- **Programmable constant resistance feed**
- **Line-feed characteristics independent of battery variations**
- **Programmable loop-detect threshold**
- **On-chip switching regulator for low-power dissipation**
- **Pin for external ground-key noise filter capacitor available**

- **Ground-key detect option available**
- **Two-wire impedance set by single external impedance**
- **Polarity reversal feature**
- **Tip Open state for ground-start lines**
- **Test relay driver optional**
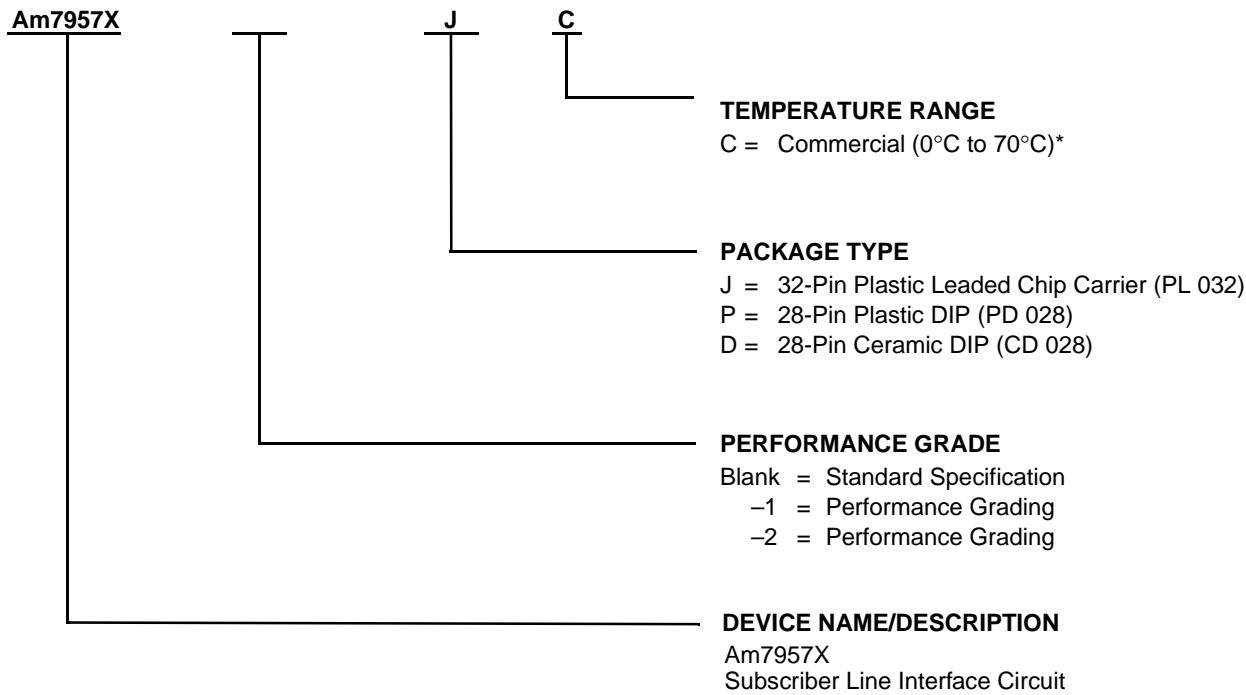- **On-hook transmission**

BLOCK DIAGRAM
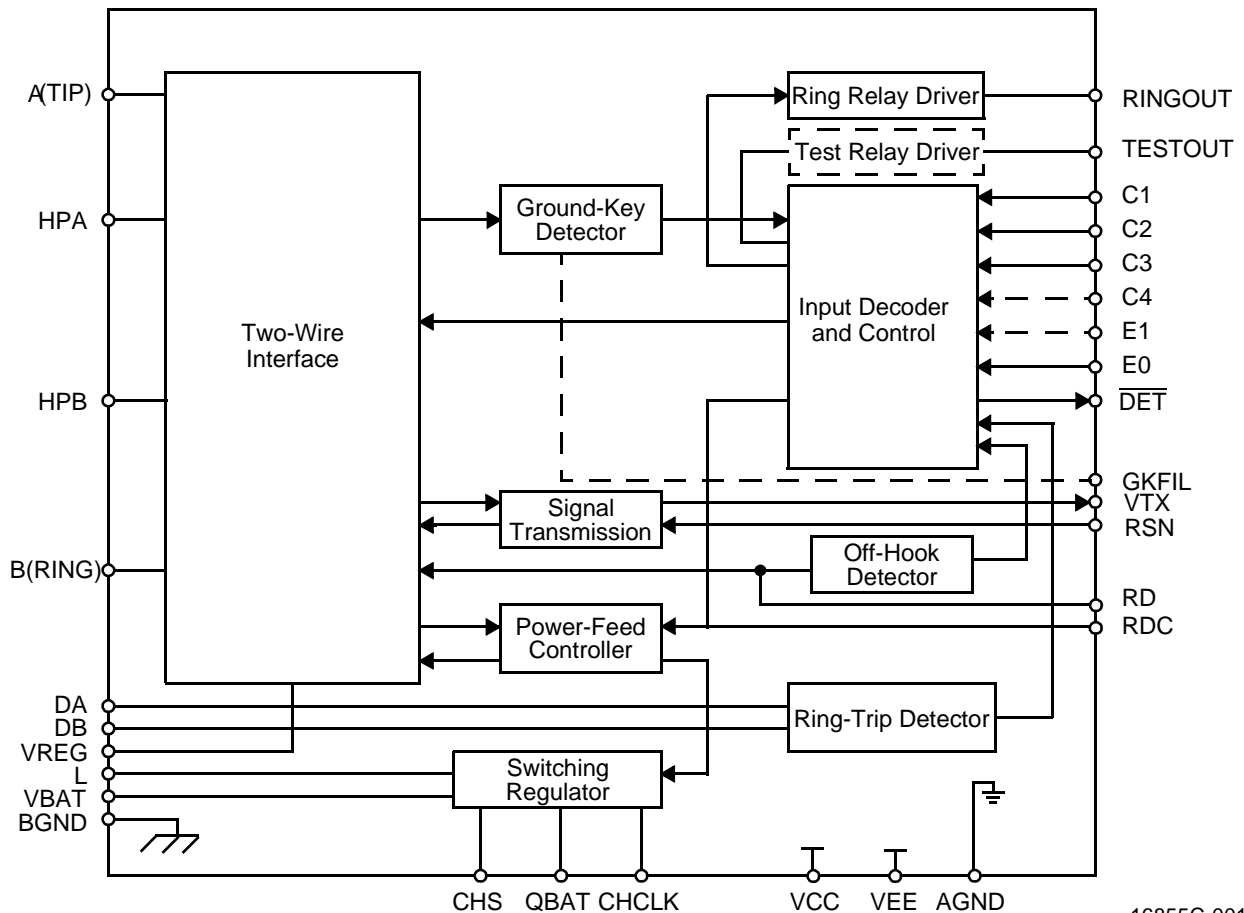
16855C-001

Notes:

1. *Am79571—E0 and E1 inputs; ring relay sourced internally to BGND; no test relay driver; ground-key filter pin.*

2. *Am79573—E0 input and no E1 input; ring and test relay drivers sourced internally to BGND.*

3. *Am79574—E0 and E1 inputs; ring and test relay drivers sourced internally to BGND.*

4. *Output amplifier current gain (K_1) = 1000 for all three parts.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am7957X   **J**   **C**

TEMPERATURE RANGE

C = Commercial (0°C to 70°C)*

PACKAGE TYPE

J = 32-Pin Plastic Leaded Chip Carrier (PL 032)
P = 28-Pin Plastic DIP (PD 028)
D = 28-Pin Ceramic DIP (CD 028)

PERFORMANCE GRADE

Blank = Standard Specification
  −1 = Performance Grading
  −2 = Performance Grading

DEVICE NAME/DESCRIPTION

Am7957X
Subscriber Line Interface Circuit

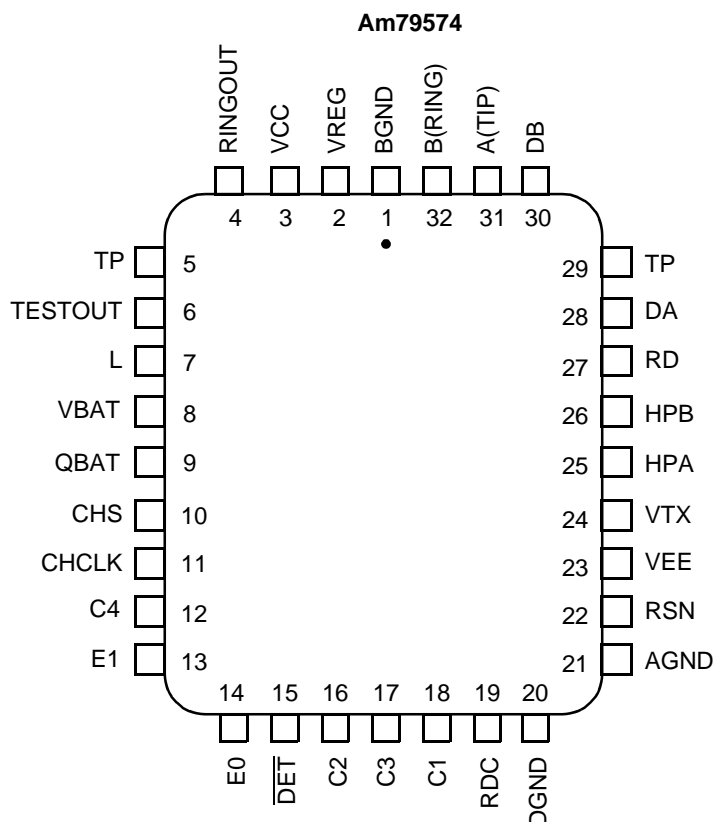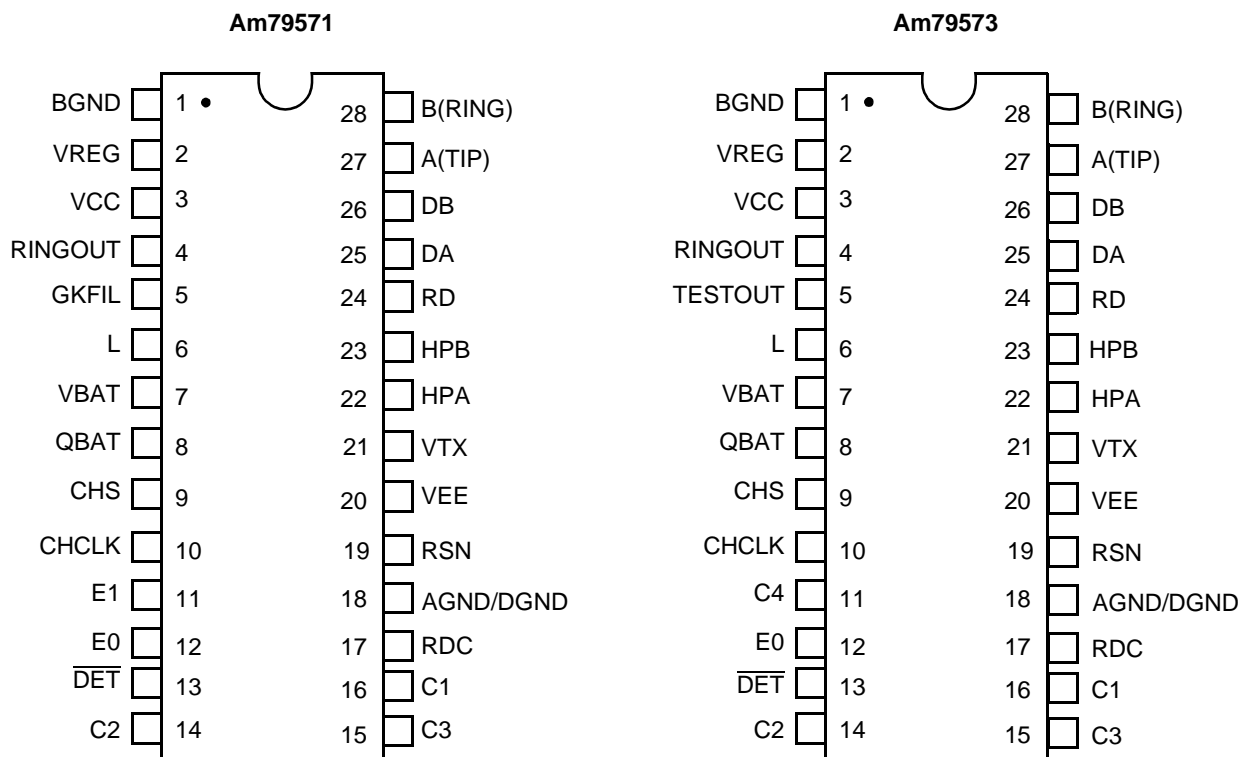| Valid Combinations		
	−1	DC
Am7957X	−2	JC
		PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note:

* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from −40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

CONNECTION DIAGRAMS

Top View

Am79571

Pin	Signal		Pin	Signal
1	BGND		28	B(RING)
2	VREG		27	A(TIP)
3	VCC		26	DB
4	RINGOUT		25	DA
5	GKFIL		24	RD
6	L		23	HPB
7	VBAT		22	HPA
8	QBAT		21	VTX
9	CHS		20	VEE
10	CHCLK		19	RSN
11	E1		18	AGND/DGND
12	E0		17	RDC
13	$\overline{\text{DET}}$		16	C1
14	C2		15	C3

Am79573

Pin	Signal		Pin	Signal
1	BGND		28	B(RING)
2	VREG		27	A(TIP)
3	VCC		26	DB
4	RINGOUT		25	DA
5	TESTOUT		24	RD
6	L		23	HPB
7	VBAT		22	HPA
8	QBAT		21	VTX
9	CHS		20	VEE
10	CHCLK		19	RSN
11	C4		18	AGND/DGND
12	E0		17	RDC
13	$\overline{\text{DET}}$		16	C1
14	C2		15	C3

Am79574

Top pins (left to right): 4 RINGOUT, 3 VCC, 2 VREG, 1 BGND, 32 B(RING), 31 A(TIP), 30 DB

Left side (top to bottom): 5 TP, 6 TESTOUT, 7 L, 8 VBAT, 9 QBAT, 10 CHS, 11 CHCLK, 12 C4, 13 E1

Right side (top to bottom): 29 TP, 28 DA, 27 RD, 26 HPB, 25 HPA, 24 VTX, 23 VEE, 22 RSN, 21 AGND

Bottom pins (left to right): 14 E0, 15 $\overline{\text{DET}}$, 16 C2, 17 C3, 18 C1, 19 RDC, 20 DGND

Notes:

1. Pin 1 is marked for orientation.

2. TP is a thermal conduction pin tied to substrate (QBAT).

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND	Gnd	(Am79574) Analog (quiet) ground
AGND/DGND	Gnd	(Am79571/Am79573) Analog and digital ground are connected internally to a single pin.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
C4	Input	(Am79573/Am79574) Test relay driver command. TTL compatible. Logic Low enables the driver.
CHCLK	Input	Chopper clock. Input to switching regulator (TTL compatible). Freq = 256 kHz (Nominal).
CHS	Input	Chopper stabilization. Connection for external stabilization components.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
DET	Output	Detector. Logic Low indicates that the selected detector is tripped. Logic inputs C3–C1, E1, and E0 select the detector. Open-collector with a built-in 15 kΩ pull-up resistor.
DGND	Gnd	(Am79574) Digital ground.
E0	Input	A logic High enables $\overline{\text{DET}}$. A logic Low disables $\overline{\text{DET}}$.
E1	Input	(Am79571/Am79574) E1 = High connects the ground-key detector to $\overline{\text{DET}}$, and E1 = Low connects the off-hook or ring-trip detector to $\overline{\text{DET}}$.
GKFIL	Capacitor	(Am79571) Ground-key filter capacitor. You can connect an external filter capacitor for filtering out high frequency noise from the ground-key loop to this pin. An internal 36 kΩ –20%, +40% resistor forms an RC filter with the external capacitor. In versions that have a GKFIL pin, connect a 3.3 nF min capacitance from the GKFIL pin to ground.
HPA	Capacitor	High-pass filter capacitor; A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor; B(RING) side of high-pass filter capacitor.
L	Output	Switching Regulator Power Transistor. Connection point for filter inductor and anode of catch diode. Has up to 60 V of pulse waveform on it and must be isolated from sensitive circuits. Keep the diode connections short because of the high currents and high di/dt.
QBAT	Battery	Filtered battery supply for the signal processing circuits.
RD	Resistor	Detector resistor. Threshold modification/filter point for the off-hook detector.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network, which also connects to the receiver summing node (RSN). V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring relay driver. Sourcing from BGND with internal diode to QBAT.
RSN	Input	The metallic current (AC and DC) between A(TIP) and B(RING) = 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
TESTOUT	Output	(Am79573/Am79574) Test relay driver. Source from BGND with internal diode to QBAT.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation
VBAT	Battery	Battery supply. Connected through an external protection diode.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VREG	Input	Regulated voltage. Provides negative power supply for power amplifiers, connection point for inductor, filter capacitor, and chopper stabilization.
VTX	Output	Transmit Audio. Unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature .... −55°C to +150°C

V_{CC} with respect to AGND/DGND...... −0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND ...... +0.4 V to −7.0 V

V_{BAT} with respect to AGND/DGND ..... +0.4 V to −70 V

Note: *Rise time of V_{BAT} (dv/dt) must be limited to 27 V/μs or less when Q_{BAT} bypass = 0.33 μF.*

BGND with respect to AGND/DGND.. +1.0 V to −3.0 V

A(TIP) or B(RING) to BGND:

    Continuous..................................... −70 V to +1.0 V
    10 ms (f = 0.1 Hz) .... −70 V to +5.0 V
    1 μs (f = 0.1 Hz) .... −90 V to +10 V
    250 ns (f = 0.1 Hz) .... −120 V to +15 V

Current from A(TIP) or B(RING)......................±150 mA

Voltage on RINGOUT ....BGND to 70 V above Q_{BAT}

Voltage on TESTOUT ....BGND to 70 V above Q_{BAT}

Current through relay drivers ....60 mA

Voltage on ring-trip inputs

    (DA and DB) .... V_{BAT} to 0 V

Current into ring-trip inputs.................................±10 mA

Peak current into regulator

    Switch (L pin) ....150 mA

Switcher transient peak off

    Voltage on L pin...+1.0 V

C4–C1, E1, CHCLK to

    AGND/DGND .... −0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, (see note) ......T_A = 70°C

    In 28-pin ceramic DIP package....................2.58 W
    In 28-pin plastic DIP package ....1.4 W
    In 32-pin PLCC package.............................1.74 W

Note: *Thermal limiting circuitry on-chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature .... 0°C to +70°C*

V_{CC} .... 4.75 V to 5.25 V

V_{EE}... −4.75 V to −5.25 V

V_{BAT} .... −40 V to −58 V

AGND/DGND... 0 V

BGND with respect to
    AGND/DGND .... −100 mV to +100 mV

Load Resistance on VTX to ground............. 10 kΩ min

Operating Ranges define those limits between which the functionality of the device is guaranteed.

* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from −40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)		Min	Typ	Max	Unit	Note
Analog (V_{TX}) output impedance				3		Ω	4
Analog (V_{TX}) output offset	0°C to 70°C		−35		+35	mV	—
		−1*	−30		+30		—
	−40°C to +85°C		−40		+40		4
		−1	−35		+35		4
Analog (RSN) input impedance				1	20	Ω	4
Longitudinal impedance at A or B	300 Hz to 3.4 kHz				35		
Overload level Z_{2WIN} = 600 to 900 Ω	4-wire 2-wire		−3.1		+3.1	Vpk	2
Transmission Performance, 2-Wire Impedance							
2-wire return loss (See Test Circuit D)	300 Hz to 500 Hz 500 Hz to 2.5 kHz 2500 Hz to 3.4 kHz		26 26 20			dB	4, 11
Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C)							
R_L = 600 Ω Longitudinal to metallic L-T, L-4	300 Hz to 3.4 kHz 300 Hz to 3.4 kHz −1*		48 52				
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz normal polarity 0°C to +70°C −2* normal polarity −40°C to +85°C −2 reverse polarity −2		63 58 54			dB	— 4 —
	1 kHz to 3.4 kHz normal polarity 0°C to +70°C −2* normal polarity −40°C to +85°C −2 reverse polarity −2		58 54 54				— 4 —
Longitudinal signal generation 4-L	300 Hz to 800 Hz 300 Hz to 800 Hz −1*		40 42				
Longitudinal current capability per wire	Active state OHT state			25 18		mArms	4
Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B)							
Gain accuracy	0 dBm, 1 kHz, 0°C to +70°C 0 dBm, 1 kHz, −40°C to +85°C 0 dBm, 1 kHz, 0°C to +70°C −1* 0 dBm, 1 kHz, −40°C to +85°C −1		−0.15 −0.20 −0.1 −0.15		+0.15 +0.20 +0.1 +0.15	dB	— 4 — 4
Variation with frequency	300 Hz to 3.4 kHz Relative to 1 kHz 0°C to +70°C −40°C to +85°C		−0.1 −0.15		+0.1 +0.15	dB	— 4
Gain tracking	+7 dBm to −55 dBm 0°C to +70°C −40°C to +85°C		−0.1 −0.15		+0.1 +0.15		— 4

Notes:

P.G. = Performance Grade

−2 grade performance parameters are equivalent to −1 performance parameters except where indicated.

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Balance Return Signal (4- to 4-Wire, See Test Circuit B)						
Gain accuracy	0 dBm, 1 kHz, 0°C to +70°C 0 dBm, 1 kHz, −40°C to +85°C 0 dBm, 1 kHz, 0°C to +70°C −1* 0 dBm, 1 kHz, −40°C to +85°C −1	−0.15 −0.20 −0.1 −0.15		+0.15 +0.20 +0.1 +0.15	dB	— 4 — 4
Variation with frequency	300 Hz to 3.4 kHz Relative to 1 kHz 0°C to +70°C −40°C to +85°C	 −0.1 −0.15		 +0.1 +0.15	dB	 — 4
Gain tracking	+7 dBm to −55 dBm 0°C to +70°C −40°C to +85°C	 −0.1 −0.15		 +0.1 +0.15		 — 4
Group delay	f = 1 kHz		5.3		µs	4
Total Harmonic Distortion (2- to 4-Wire or 4- to 2-Wire, See Test Circuits A and B)						
Total harmonic distortion	0 dBm, 300 Hz to 3.4 kHz +9 dBm, 300 Hz to 3.4 kHz		−64 −55	−50 −40	dB	
Idle Channel Noise						
C-message weighted noise	2-wire, 0°C to +70°C 2-wire, 0°C to +70°C −1* 2-wire, −40°C to +85°C		+7 +7 +7	+15 +12 +15	dBrnc	— — 4
	4-wire, 0°C to +70°C 4-wire, 0°C to +70°C −1* 4-wire, −40°C to +85°C		+7 +7 +7	+15 +12 +15		— — 4
Psophometric weighted noise	2-wire, 0°C to +70°C 2-wire, 0°C to +70°C −1* 2-wire, −40°C to +85°C		−83 −83 −83	−75 −78 −75	dBmp	7 — 4, 7
	4-wire, 0°C to +70°C 4-wire, 0°C to +70°C −1* 4-wire, −40°C to +85°C		−83 −83 −83	−75 −78 −75		7 — 4, 7
Single Frequency Out-of-Band Noise (See Test Circuit E)						
Metallic	4 kHz to 9 kHz 9 kHz to 1 MHz 256 kHz and harmonics		−76 −76 −57		dBm	4, 5, 9 4, 5, 9 4, 5
Longitudinal	1 kHz to 15 kHz Above 15 kHz 256 kHz and harmonics		−70 −85 −57			4, 5, 9 4, 5, 9 4, 5
Line Characteristics (See Figure 1) BAT = −48 V, R_L = 600 Ω and 900 Ω, R_{FEED} = 800 Ω						
Apparent battery voltage	Active state	47	50	53	V	
Loop current accuracy	Active state	−7.5		+7.5	%	
Loop current—Tip Open	R_L = 600 Ω			1.0	mA	
Loop current—Open Circuit	R_L = 0 Ω			1.0		
Loop current limit accuracy	OHT state Active state	−20		+20	%	10
Fault current limit, I_LLIM (I_{AX} + I_{BX})	A and B shorted to GND			130	mA	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Power Dissipation, BAT = –48 V, Normal Polarity						
On-hook Open Circuit state			35	120	mW	
	–1*		35	80		
On-hook OHT state			135	250		
	–1*		135	200		
On-hook Active state			200	400		
	–1*		200	300		
Off-hook OHT state	R_L = 600 Ω		500	750		
Off-hook Active state	R_L = 600 Ω		650	1000		
Supply Currents						
V_{CC} on-hook supply current	Open Circuit state OHT state Active state		3.0 6.0 8.0	4.5 10.0 13.0	mA	
V_{EE} on-hook supply current	Open Circuit state OHT state Active state		1.0 2.3 3.0	2.3 3.7 6.0		
V_{BAT} on-hook supply current	Open Circuit state OHT state Active state		0.4 3.2 4.5	1.0 5.5 7.0		
Power Supply Rejection Ratio (V_{RIPPLE} = 50 mVrms)						
V_{CC}	50 Hz to 3.4 kHz	25	45		dB	6, 7
	–1*	30	45			
	3.4 kHz to 50 kHz	22	35			
	–1*	25	40			
V_{EE}	50 Hz to 3.4 kHz	20	40			
	–1*	25	40			
	3.4 kHz to 50 kHz	10	25			
	–1*	10	25			
V_{BAT}	50 Hz to 3.4 kHz	27	45			
	–1*	30	45			
	3.4 kHz to 50 kHz	20	40			
	–1*	25	40			
Off-Hook Detector						
Current threshold accuracy	I_{DET} = 365/R_D Nominal	–20		+20	%	
Ground-Key Detector Thresholds, Active State, BAT = –48 V (See Test Circuit F)						
Ground-key resistance threshold	B(RING) to GND	2.0	5.0	10.0	kΩ	
Ground-key current threshold	B(RING) to GND		9		mA	8
	Midpoint to GND		9			
Ring-Trip Detector Input						
Bias current		–5	–0.05		µA	
Offset voltage	Source resistance 0 Ω to 2 MΩ	–50	0	+50	mV	12
Logic Inputs (C4–C1, E0, E1, and CHCLK)						
Input High voltage		2.0			V	
Input Low voltage				0.8		
Input High current	All inputs except E1	–75		40	µA	
Input High current	Input E1	–75		45		
Input Low current		–0.4			mA	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Logic Output (DET)						
Output Low voltage	I_{OUT} = 0.8 mA			0.4	V	
Output High voltage	I_{OUT} = −0.1 mA	2.4			V	
Relay Driver Outputs (RINGOUT, TESTOUT)						
On voltage	50 mA source	BGND − 2	BGND −.95		V	
Off leakage			0.5	100	µA	
Clamp voltage	50 mA sink	Q_{BAT} −2			V	

RELAY DRIVER SCHEMATICS

Am79571/Am79573/Am79574 — BGND — RINGOUT — Q_{BAT}

Am79573/Am79574 — BGND — TESTOUT — Q_{BAT}
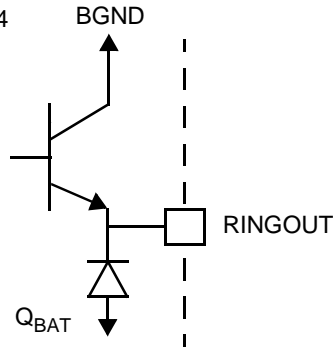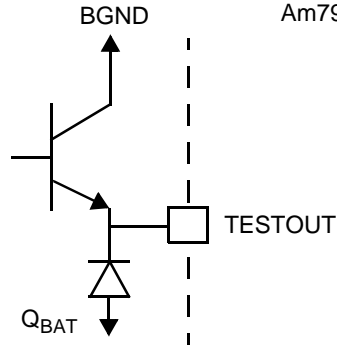
SWITCHING CHARACTERISTICS

Am79571/Am79573/Am79574

Symbol	Parameter	Test Conditions	Temperature Range	Min	Typ	Max	Unit	Note
*tgkde	E1 Low to DET High (E0 = 1)		0°C to +70°C −40°C to +85°C			3.8 4.0		
	E1 Low to DET Low (E0 = 1)	Ground-Key Detect state R_L open, R_G connected (See Figure H)	0°C to +70°C −40°C to +85°C			1.1 1.6		
tgkdd	E0 High to DET Low (E1 = 0)		0°C to +70°C −40°C to +85°C			1.1 1.6		
tgkd0	E0 Low to DET High (E1 = 0)		0°C to +70°C −40°C to +85°C			3.8 4.0	µs	4
*tshde	E1 High to DET Low (E0 = 1)		0°C to +70°C −40°C to +85°C			1.2 1.7		
	E1 High to DET High (E0 = 1)	Switchhook Detect state R_L = 600 Ω, R_G open (See Figure G)	0°C to +70°C −40°C to +85°C			3.8 4.0		
*tshdd	E0 High to DET Low (E1 = 1)		0°C to +70°C −40°C to +85°C			1.1 1.6		
*tshd0	E0 Low to DET High (E1 = 1)		0°C to +70°C −40°C to +85°C			3.8 4.0		

Note:

This parameter is not applicable to the Am79573. E1 is internally connected to a logical 0.

SWITCHING WAVEFORMS

Am79571/Am79573/Am79574

E1 to $\overline{\text{DET}}$*
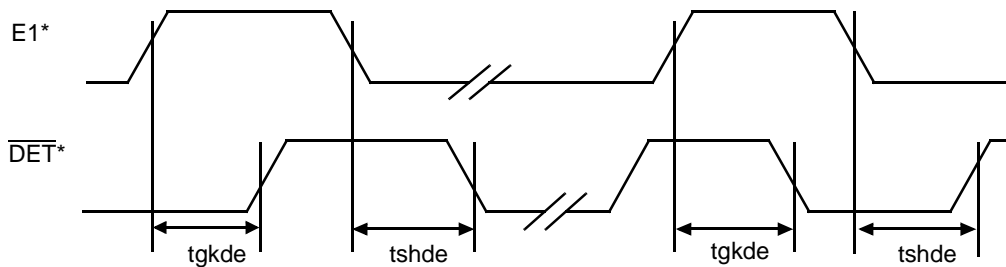
E0 to $\overline{\text{DET}}$
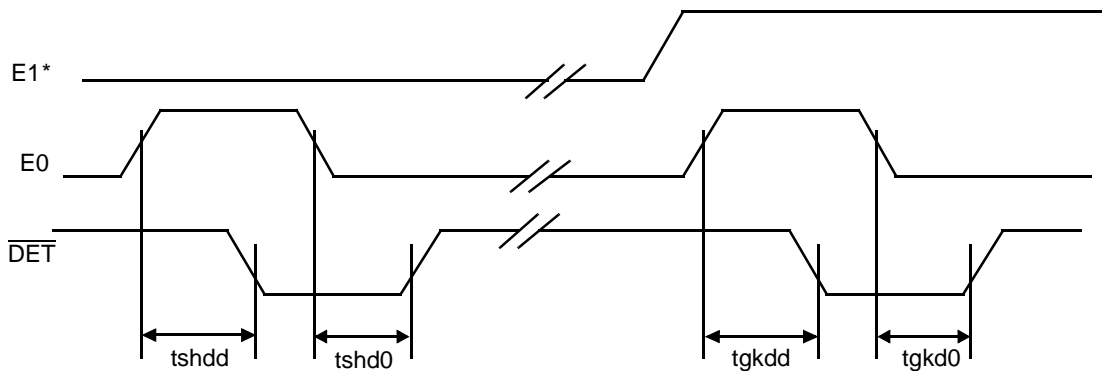
Notes:

*   This waveform is not applicable to the Am79573. E1 is internally connected to a logical 0.

1. All delays measured at 1.4 V level.

Notes:

1. Unless otherwise noted, test conditions are BAT = –48 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, C_{HP} = 0.22 μF, $R_{DC1} = R_{DC2}$ = 20 kΩ, C_{DC} = 0.1 μF, R_d = 51.1 kΩ, no fuse resistors, two-wire AC output impedance, programming impedance (Z_T) = 600 kΩ resistive, receive input summing impedance (Z_{RX}) = 300 kΩ resistive. (See Table 2 for component formulas.)

2. Overload level is defined when THD = 1%.

3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire AC load impedance matches the impedance programmed by Z_T.

4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.

5. These tests are performed with a longitudinal impedance of 90 Ω and metallic impedance of 300 Ω for frequencies below 12 kHz and 135 Ω for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout.

6. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.

7. When the SLIC is in the anti-sat 2 operating region, this parameter is degraded. The exact degradation depends on system design. The anti-sat 2 region occurs at high loop resistances when $|V_{BAT}| - |V_{AX} - V_{BX}|$ is less than 14 V.

8. Midpoint is defined as the connection point between two 300 Ω series resistors connected between A(TIP) and B(RING).

9. Fundamental and harmonics from 256 kHz switch-regulator chopper are not included.

10. Calculate loop-current limit using the following equations:

In OHT state: $\quad I_{LIMIT} = 0.5 \dfrac{V_{APPARENT}}{R_{FEED}}$

In Active state: $\quad I_{LIMIT} = 0.8 \dfrac{V_{APPARENT}}{R_{FEED}}$

11. Assumes the following Z_T network:

```
VTX ──/\/\/── ──/\/\/── RSN
      300 kΩ  │  300 kΩ
              │
             ═╪═
              │
              ▽
            30 pF
```
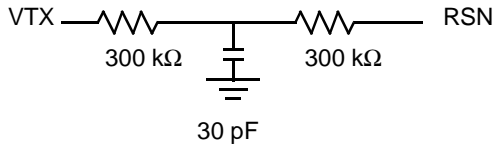
12. Tested with 0 Ω source impedance. 2 MΩ is specified for system design purposes only.

13. Group delay can be considerably reduced by using a Z_T network such as that shown in Note 11 above. The network reduces the group delay to less than 2 μs. The effect of group delay on linecard performance may be compensated for by using QSLAC™ or DSLAC™ devices.

Table 1. SLIC Decoding

State	C3 C2 C1	Two-Wire Status	$\overline{DET}$ Output E0 = 1* E1 = 0**	$\overline{DET}$ Output E0 = 1* E1 = 1**
0	0 0 0	Open Circuit	Ring trip	Ring trip
1	0 0 1	Ringing	Ring trip	Ring trip
2	0 1 0	Active	Loop detector	Ground key
3	0 1 1	On-hook TX (OHT)	Loop detector	Ground key
4	1 0 0	Tip Open	Loop detector	—
5	1 0 1	Reserved	Loop detector	—
6	1 1 0	Active Polarity Reversal	Loop detector	Ground key
7	1 1 1	OHT Polarity Reversal	Loop detector	Ground key

Notes:

*   A logic Low on E0 disables the $\overline{DET}$ output into the Open Collector state.

** For the Am79573, E1 is internally connected to a logical 0.

Table 2. User-Programmable Components

|	
$Z_T = 1000(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \dfrac{Z_L}{G_{42L}} \bullet \dfrac{1000 \bullet Z_T}{Z_T + 1000(Z_L + 2R_F)}$	Z_{RX} is connected from VRX to the RSN pin, Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = 50(R_{FEED} - 2R_F)$ $C_{DC} = 1.5 \text{ ms} \bullet \dfrac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = \dfrac{365}{I_T}, \qquad C_D = \dfrac{0.5 \text{ ms}}{R_D}$	R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on hook and off hook.

DC FEED CHARACTERISTICS

$V_{BAT} = -47.3$ V
$R_{DC} = 40$ kΩ

——— Active state
– – – – OHT state
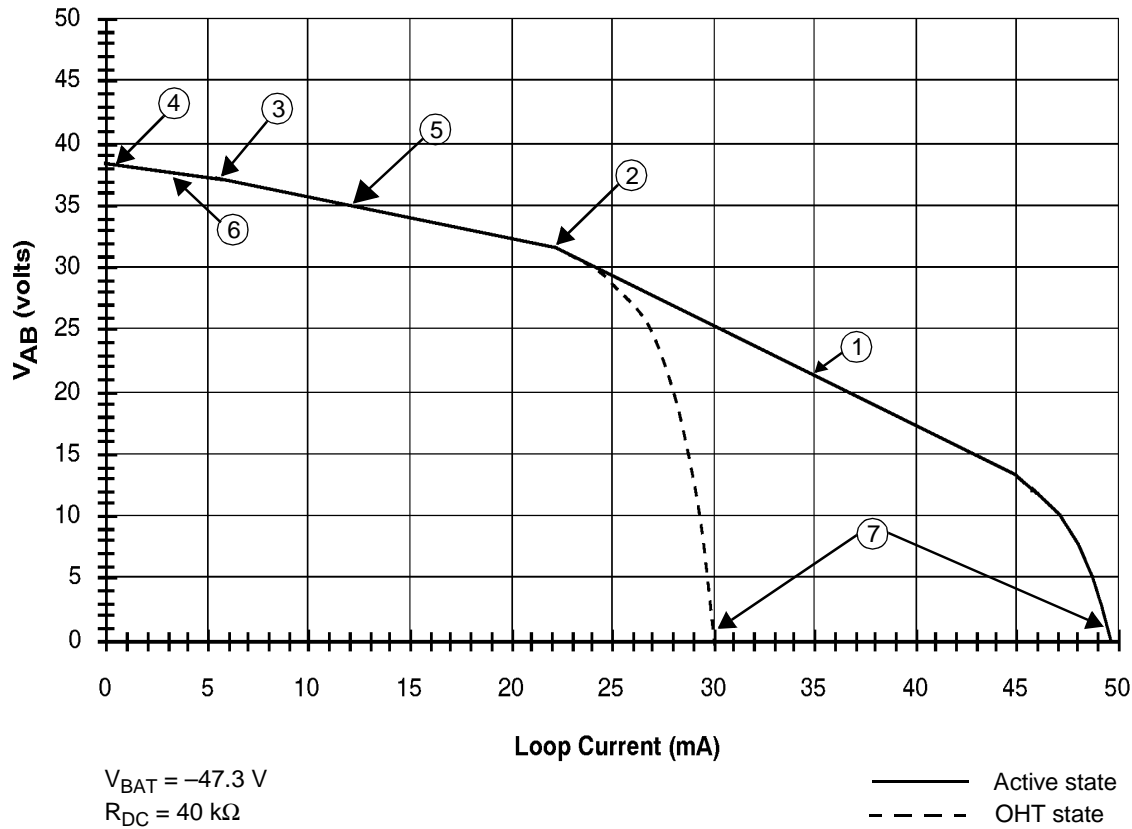
Notes:

1. *Constant-resistance feed region:* $V_{AB} = 50 - I_L\left(\dfrac{R_{DC}}{50}\right)$

2. *Anti-sat –1 turn-on:* $V_{AB} = 31.8$ V

3. *Anti-sat –2 turn-on:* $V_{AB} = 1.077|V_{BAT}| - 12.538$

4. *Open circuit voltage:* $V_{AB} = 0.377|V_{BAT}| + 20.48,$ $|V_{BAT}| < 50.2$ V
   $V_{AB} = 39.39$ V $|V_{BAT}| \geq 50.2$ V

5. *Anti-sat –1 region:* $V_{AB} = 39.39 - I_L\left(\dfrac{R_{DC}}{118.3}\right)$

6. *Anti-sat –2 region:* $V_{AB} = 0.377|V_{BAT}| + 20.48 - I_L\left(\dfrac{R_{DC}}{200}\right)$

7. *Current Limit:*
   Active state, $I_L = 0.8\left(\dfrac{2500}{R_{DC}}\right)$

   OHT state, $I_L = 0.5\left(\dfrac{2500}{R_{DC}}\right)$

a. V_A–V_B (V_{AB}) Voltage vs. Loop Current (Typical)

DC FEED CHARACTERISTICS (continued)
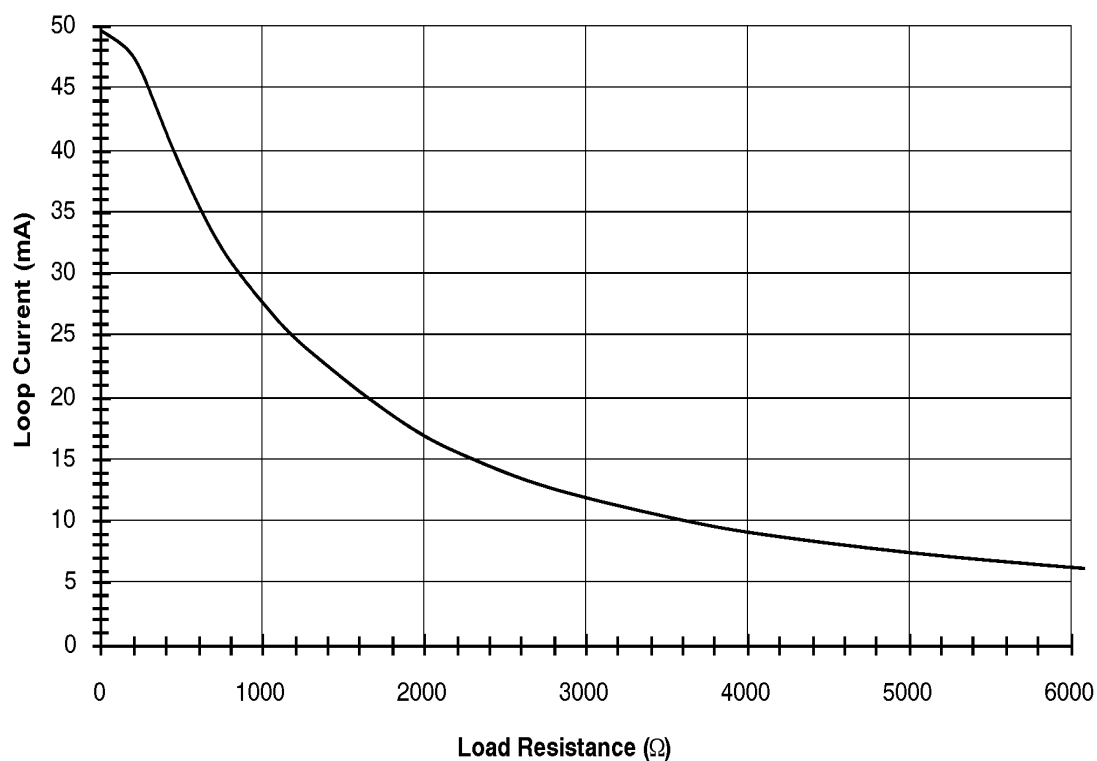
$V_{BAT} = -47.3$ V
$R_{DC} = 40$ kΩ

b. Loop Current vs. Load Resistance (Typical)
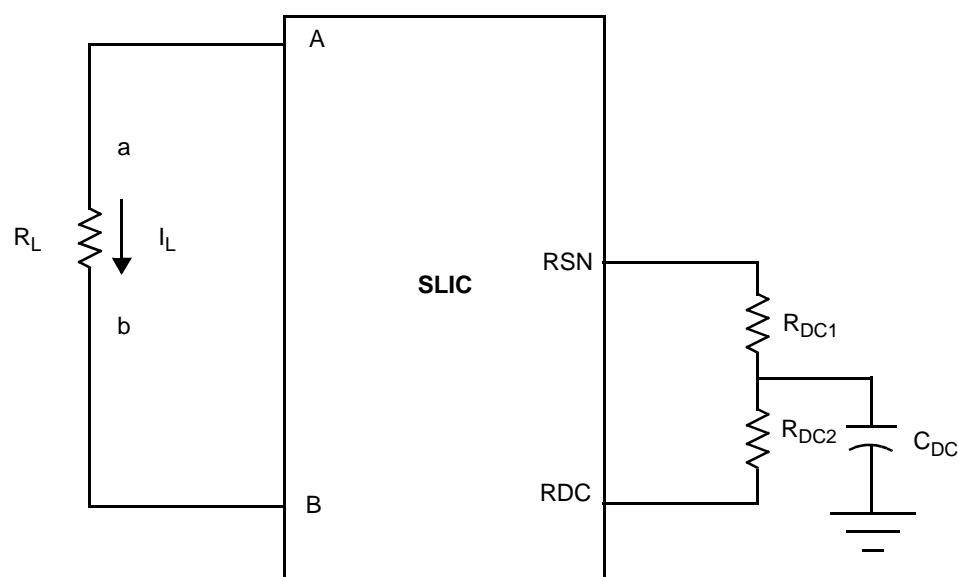
Feed resistance programmed by R_{DC1} and R_{DC2}

c. Feed Programming

Figure 1. DC Feed Characteristics

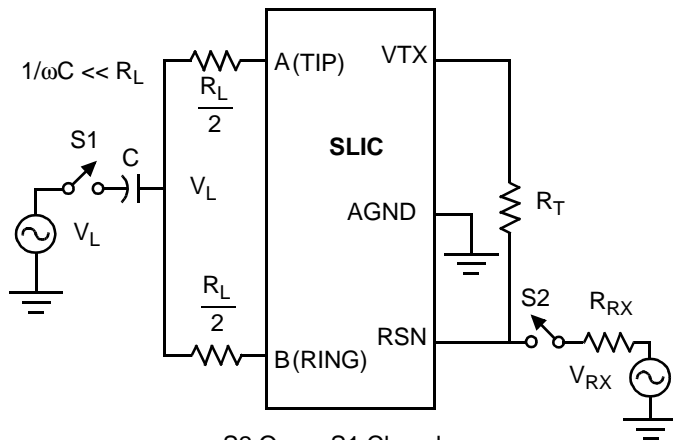## TEST CIRCUITS
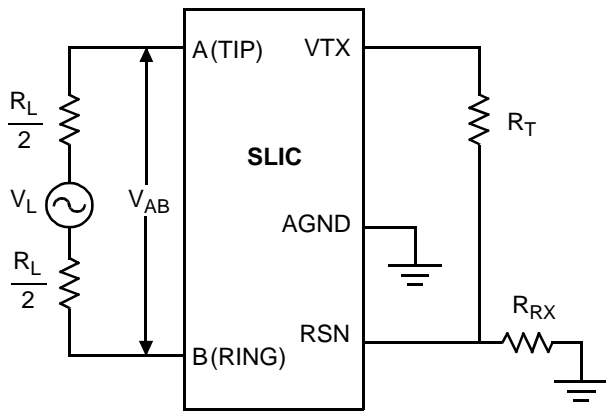
$$I_{L2-4} = -20 \log (V_{TX} / V_{AB})$$

A. Two- to Four-Wire Insertion Loss
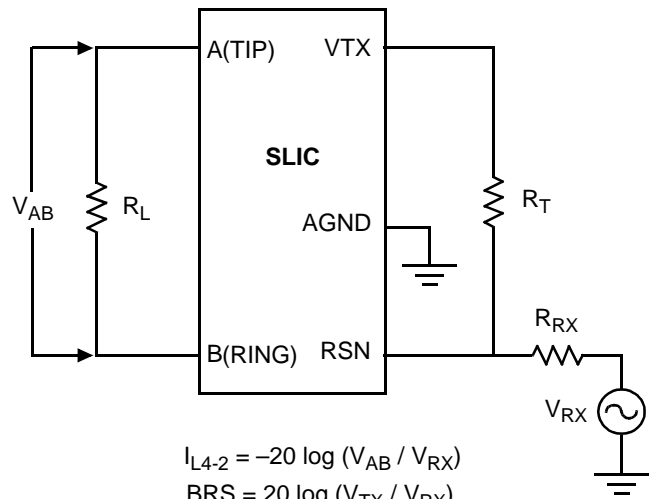
$$I_{L4-2} = -20 \log (V_{AB} / V_{RX})$$
$$BRS = 20 \log (V_{TX} / V_{RX})$$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal

S2 Open, S1 Closed:

L-T Long. Bal. = $20 \log (V_{AB} / V_L)$

L-4 Long. Bal. = $20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open:

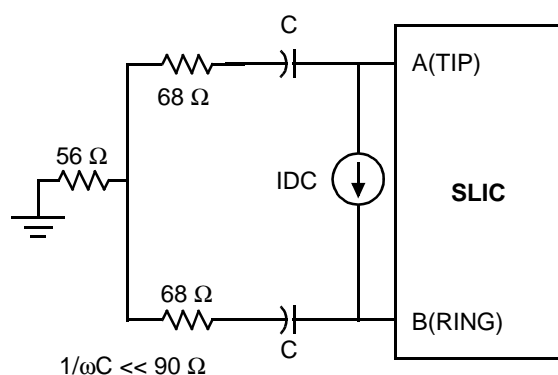4-L Long. Sig. Gen. = $20 \log (V_L / V_{RX})$

C. Longitudinal Balance
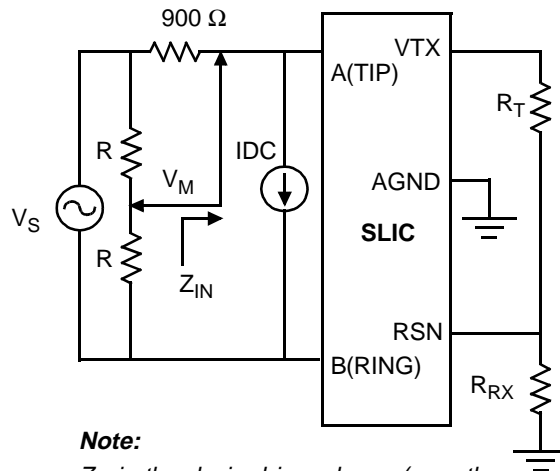
Note:

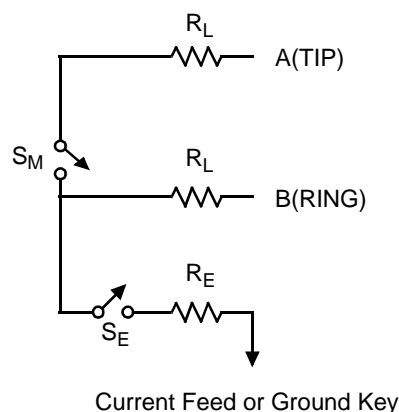Z_D is the desired impedance (e.g., the characteristic impedance of the line).

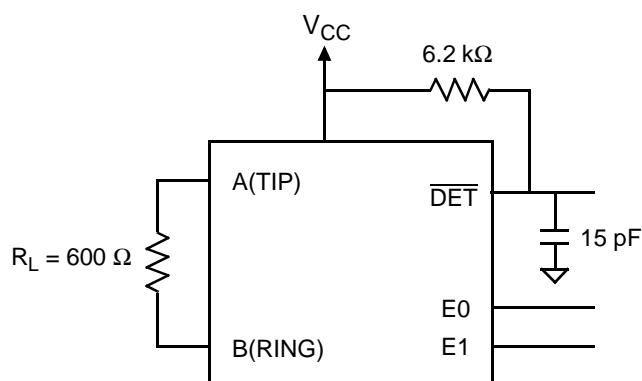$R_L = -20 \log (2 V_M / V_S)$

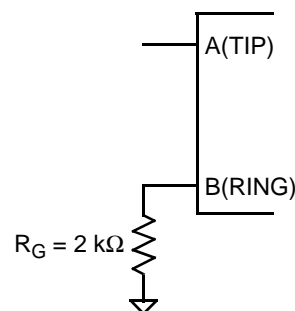**D. Two-Wire Return Loss Test Circuit**

TEST CIRCUITS (continued)

C

68 Ω

56 Ω

IDC

SLIC

A(TIP)

B(RING)

68 Ω

C

$1/\omega C \ll 90\ \Omega$

E. Single-Frequency Noise

R_L A(TIP)

S_M

R_L B(RING)

R_E

S_E

Current Feed or Ground Key

F. Ground-Key Detection

V_{CC}

6.2 kΩ

A(TIP) $\overline{DET}$

$R_L = 600\ \Omega$

15 pF

B(RING)   E0

E1

G. Loop-Detector Switching

A(TIP)

B(RING)

$R_G = 2\ k\Omega$

H. Ground-Key Switching

REVISION SUMMARY

Revision B to Revision C

• Minor changes were made to the data sheet style and format to conform to AMD standards.

Revision C to Revision D

• In Pin Description table, inserted/changed TP pin description to: "Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation."

• Minor changes were made to the data sheet style and format to conform to AMD standards.